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PATENT  
Attorney Docket No. ASC-012DV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):        *Lee et al.*  
SERIAL NO.:         10/788,741                      GROUP NO.:         2813  
FILING DATE:        February 27, 2004      EXAMINER:         Craig Thompson  
TITLE:                STRUCTURES WITH PLANAR STRAINED LAYERS

**CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8**

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 23<sup>rd</sup> day of March, 2005.

*Wendy L. Martin*  
Wendy L. Martin

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Submitted herewith are:

1. Transmittal Form (1 page);
2. Supplemental Information Disclosure Statement (2 pages);
3. PTO Form 1449 (4 pages);
4. Copies of cited references (C75 – C95); and
5. Return receipt postcard



# TRANSMITTAL FORM

Application Serial Number	10/788,741
Filing Date	February 27, 2004
First Named Inventor	Lee
Group Art Unit	2813
Examiner Name	Craig Thompson
Attorney Docket No.	ASC-012DV
Patent No.	Not applicable
Issue Date	Not applicable

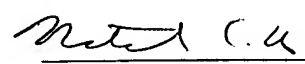
## ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Check Attached <input type="checkbox"/> Copy of Fee Transmittal Form	<input type="checkbox"/> Copy of Notice to File Missing Parts of Application <input type="checkbox"/> Formal Drawing(s) <input type="checkbox"/> Request For Continued Examination (RCE) Transmittal <input type="checkbox"/> Power of Attorney (Revocation of Prior Powers) <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Executed Declaration and Power of Attorney for Utility or Design Patent Application <input type="checkbox"/> Small Entity Statement <input type="checkbox"/> CD(s) for large table or computer program <input type="checkbox"/> Amendment After Allowance <input type="checkbox"/> Request for Certificate of Correction <input type="checkbox"/> Certificate of Correction (in duplicate)	<input type="checkbox"/> Notice of Appeal to Board of Patent Appeals and Interferences <input type="checkbox"/> Appeal Brief (in triplicate) <input type="checkbox"/> Status Inquiry <input checked="" type="checkbox"/> Return Receipt Postcard <input checked="" type="checkbox"/> Certificate of First Class Mailing under 37 C.F.R. 1.8 <input type="checkbox"/> Certificate of Facsimile Transmission under 37 C.F.R. 1.8 <input type="checkbox"/> Additional Enclosure(s) (please identify below)
<input type="checkbox"/> Amendment/Response <input type="checkbox"/> Preliminary <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Letter to Official Draftsperson including Drawings [Total Sheets ____]		
<input type="checkbox"/> Petition for Extension of Time		
<input checked="" type="checkbox"/> Supplemental Information Disclosure Statement <input checked="" type="checkbox"/> Form PTO-1449 <input checked="" type="checkbox"/> Copies of IDS Citations (C75 - C95)		
<input type="checkbox"/> Certified Copy of Priority Document(s)		
<input type="checkbox"/> Sequence Listing submission <input type="checkbox"/> Paper Copy/CD <input type="checkbox"/> Computer Readable Copy <input type="checkbox"/> Statement verifying identity of above		

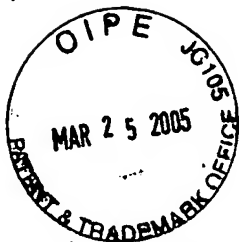
## CORRESPONDENCE ADDRESS

Direct all correspondence to: Patent Administrator  
Goodwin Procter LLP  
Exchange Place  
Boston, MA 02109  
Tel. No.: (617) 570-1000  
Fax No.: (617) 523-1231  
Customer No. 051414

## SIGNATURE BLOCK

Respectfully submitted,  
  
Natasha C. Us  
Attorney for Applicant(s)  
Goodwin Procter LLP  
Exchange Place  
Boston, MA 02109

Date: March 23, 2005  
Reg. No. 44,381  
Tel. No.: (617) 570-1806  
Fax No.: (617) 523-1231



PATENT  
Attorney Docket No. ASC-012DV

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APPLICANT(S): Lee *et al.*  
SERIAL NO.: 10/788,741 GROUP NO.: 2813  
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TITLE: STRUCTURES WITH PLANAR STRAINED LAYERS

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98(a)(2)(i), only copies of the non-patent publications are enclosed.

REMARKS

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- ☒ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- ☐ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and
- ☐ the requisite Statement is below, **OR**
- ☐ the requisite fee under 37 C.F.R. 1.17(p), namely **\$180.00**, is included herein, or

- ☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee**, **AND**
- ☐ the requisite Statement is below, **AND**
- ☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

#### STATEMENT

As required under 37 C.F.R. 1.97(e), Applicant(s), through the undersigned, hereby state either that [check the appropriate space only if either (2) or (3) is checked on the previous page and the Statement is required]:

- ☐ 1. Each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application **not more than three months** prior to the filing of the Information Disclosure Statement; or
- ☐ 2. No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this Statement after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to **any individual** designated in 37 C.F.R. 1.56(c) **more than three months** prior to the filing of the Information Disclosure Statement.

Respectfully submitted,



Natasha C. Us  
Attorney for Applicant(s)  
Goodwin Procter LLP  
Exchange Place  
Boston, Massachusetts 02109  
Customer No. 051414

Date: March 23, 2005  
Reg. No. 44,381

Tel. No.: (617) 570-1806  
Fax No.: (617) 523-1231  
VER 12/00



FORM PTO - 1449

SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT

ATTORNEY DOCKET NO.: ASC-012DV

APPLICANT(S): Lee *et al.*

SERIAL NO.: 10/788,741

FILING DATE: February 27, 2004

GROUP: 2813

## U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A75	2002/0063292	05/30/2002	Armstrong <i>et al.</i>			
	A76	2002/0190284	12/19/2002	Murthy <i>et al.</i>			
	A77	2004/0007724	01/15/2004	Murthy <i>et al.</i>			
	A78	2004/0014276	01/22/2004	Murthy <i>et al.</i>			
	A79	2004/0070035	04/15/2004	Murthy <i>et al.</i>			
	A80	2004/0084735	05/06/2004	Murthy <i>et al.</i>			
	A81	2004/0119101	06/24/2004	Schrom <i>et al.</i>			
	A82	2004/0142545	07/22/2004	Ngo <i>et al.</i>			
	A83	2004/0173815	09/09/2004	Yeo <i>et al.</i>			
	A84	5,089,872	02/18/1992	Ozturk <i>et al.</i>			
	A85	5,242,847	09/07/1993	Ozturk <i>et al.</i>			
	A86	6,228,694	05/08/2001	Doyle <i>et al.</i>			
	A87	6,235,568	05/22/2001	Murthy <i>et al.</i>			
	A88	6,281,532	08/28/2001	Doyle <i>et al.</i>			
	A89	6,326,664	12/04/2001	Chau <i>et al.</i>			
	A90	6,563,152	05/13/2003	Roberds <i>et al.</i>			
	A91	6,605,498	08/12/2003	Murthy <i>et al.</i>			
	A92	6,621,131	09/16/2003	Murthy <i>et al.</i>			
	A93	6,657,223	12/02/2003	Wang <i>et al.</i>			
	A94	6,703,648	03/09/2004	Xiang <i>et al.</i>			
	A95	6,743,684	06/01/2004	Liu			
EXAMINER				DATE CONSIDERED			

<b>FORM PTO – 1449</b>  <b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT</b>				ATTORNEY DOCKET NO.: ASC-012DV  APPLICANT(S): Lee <i>et al.</i>  SERIAL NO.: 10/788,741  FILING DATE: February 27, 2004  GROUP: 2813					
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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C75	Gannavaram, <i>et al.</i> , "Low Temperature ( $\leq 800^{\circ}\text{C}$ ) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> , (2000), pp. 437-440.							
	C76	Ge <i>et al.</i> , "Process-Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2003) pp. 73-76.							
	C77	Ghani <i>et al.</i> , "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2003), 978-980.							
	C78	Hamada <i>et al.</i> , "A New Aspect of Mechanical Stress Effects in Scaled MOS Devices," <u>IEEE Transactions on Electron Devices</u> , Vol. 38, No. 4 (April 1991), pp. 895-900.							
	C79	Huang <i>et al.</i> , "Isolation Process Dependence of Channel Mobility in Thin-Film SOI Devices," <u>IEEE Electron Device Letters</u> , Vol. 17, No. 6 (June 1996), pp. 291-293.							
	C80	Huang <i>et al.</i> , "LOCOS-Induced Stress Effects on Thin-Film SOI Devices," <u>IEEE Transactions on Electron Devices</u> , Vol. 44, No. 4 (April 1997), pp. 646-650.							
	C81	Huang, <i>et al.</i> , "Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $\text{Si}_{1-x}\text{Ge}_x$ Source/Drain", <u>IEEE Electron Device Letters</u> , Vol. 21, No. 9, (Sept. 2000) pp. 448-450.							
	C82	Iida <i>et al.</i> , "Thermal behavior of residual strain in silicon-on-insulator bonded wafer and effects on electron mobility," <u>Solid-State Electronics</u> , Vol. 43 (1999), pp. 1117-1120.							
EXAMINER					DATE CONSIDERED				

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EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C83	Ito <i>et al.</i> , "Mechanical Stress Effect on Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2000), pp. 247-250.							
	C84	Lochtefeld <i>et al.</i> , "Investigating the Relationship Between Electron Mobility and Velocity in Deeply Scaled NMOS via Mechanical Stress," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 12 (2001), pp. 591-593.							
	C85	Ootsuka <i>et al.</i> , "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Applications," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2000), pp. 575-578.							
	C86	Ota <i>et al.</i> , "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2002), pp. 27-30.							
	C87	Öztürk, <i>et al.</i> , "Advanced Si <sub>1-x</sub> Ge <sub>x</sub> Source/Drain and Contact Technologies for Sub-70 nm CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> , (2002), pp. 375-378.							
	C88	Öztürk, <i>et al.</i> , "Low Resistivity Nickel Germanosilicide Contacts to Ultra-Shallow Si <sub>1-x</sub> Ge <sub>x</sub> Source/Drain Junctions for Nanoscale CMOS," <u>IEEE International Electron Device Meeting Technical Digest</u> (2003), pp. 497-500.							
	C89	Öztürk, <i>et al.</i> , "Selective Silicon-Germanium Source/Drain Technology for Nanoscale CMOS," <u>Mat. Res. Soc. Symp. Proc.</u> , Vol. 717, (2002), pp. C4.1.1-C4.1.12.							
	C90	Öztürk, <i>et al.</i> , "Ultra-Shallow Source/Drain Junctions for Nanoscale CMOS Using Selective Silicon-Germanium Technology," <u>Extended Abstracts of International Workshop on Junction Technology</u> , (2001), pp. 77-82.							
EXAMINER					DATE CONSIDERED				

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EXAM. INIT.	<b>OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)</b>								
	C91	Shimizu <i>et al.</i> , "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2001), pp. 433-436.							
	C92	Thompson <i>et al.</i> , "A Logic Nanotechnology Featuring Strained-Silicon," <u>IEEE Electron Device Letters</u> , Vol. 25, No. 4 (April 2004), pp. 191-193.							
	C93	Thompson <i>et al.</i> , "A 90 nm Logic Technology Featuring 50nm Strained-Silicon Channel Transistors, 7 layers of Cu <i>Interconnects</i> , Low k ILD, and 1um <sup>2</sup> SRAM Cell," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (2002), pp. 61-64.							
	C94	Tiwari <i>et al.</i> , "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," <u>IEEE International Electron Devices Meeting Technical Digest</u> , (1997), pp. 939-941.							
	C95	Uchino, <i>et al.</i> , "A Raised Source/Drain Technology Using In-situ P-doped SiGe and B-doped Si for 0.1-μm CMOS ULSIs," <u>IEEE International Electron Device Meeting Technical Digest</u> , (1997), pp. 479-482.							
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				